Electrical Engineering Technical Journal, ISSN: ISSN: 3007-9772, Vol. 3, No. 1, 2026 (In press), Pages 1-7
DOI: https://doi.org/10.51173/eetj.v3i1.29

Electrical Engineering Technical Journal
Journal homepage: http://eetj.mtu.edu.iq

RESEARCH ARTICLE

$SiO_2/Al_2O_3/HfO_2$ Selective Buried Oxide Layer (SELBOX) Engineering and Its Influence on 20 nm n-MOSFET

Aemen Qais A. Al-Yozbakee [1*], Qais Th. Algwari [1]

[1] College of Electronics Engineering, Ninevah University, Mosul, Iraq

[*] Corresponding Author Email: aeman.qais.eng23@stu.uoninevah.edu.iq

Article Info.

Article history:

Received
24 July 2025

Accepted
8 October 2025

Published in Journal
5 December 2025

Abstract

Short channel effects (SCEs) provide a significant problem in the miniaturization of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) to the nanoscale. These effects impair device performance by elevating leakage currents (I_{OFF}), diminishing threshold voltage (V_{TH}) stability, and decreasing breakdown voltage. To solve these issues, various structural and material engineering strategies have been suggested, notably the implementation of a selective buried oxide layer (SELBOX) layer, which has demonstrated significant potential. This work examines the effect of SELBOX introduction on the electrical performance of nano-scaled n-MOSFETs using device simulation. A 20 nm n-MOSFET featuring a high-k HfO_2 gate dielectric was simulated utilizing the Technology Computer Aided Design (TCAD) Silvaco ATLAS software. The SELBOX layer was integrated beneath the drain region at a depth of 30 nm, with three distinct dielectric materials: SiO_2, Al_2O_3, and HfO_2 evaluated as the SELBOX substrate. To investigate the impact of the SELBOX position, its depth was adjusted from 30 nm below the drain to direct contact with the channel. A comparison examination was conducted between the standard MOSFET design (without SELBOX) and the modified devices incorporating SELBOX at different depths. The findings indicate that the dielectric constant and band gap of the implanted material, as well as its closeness to the drain and channel region, substantially influence device performance. In the instance of SiO_2 as SELBOX material, the I_{OFF} decreased by 33%, and the breakdown voltage significantly increased from 85.09 V to 491.4 V. The utilization of Al_2O_3 resulted in a 27% reduction in I_{OFF} and an increase in breakdown voltage from 85.09 V to 275.7 V. Notably, the application of HfO_2 as SELBOX material resulted in a divergent effect: I_{OFF} rose by 21%, but the breakdown voltage increased to 172.3 V.

 Publisher: Middle Technical University

Keywords: Al_2O_3, HfO_2, n-MOSFET; SELBOX; Silvaco ATLAS; Breakdown Voltage.

1. Introduction

The MOSFET continues to be fundamental to integrated circuits because of its scalability, cost efficiency, and compatibility with CMOS technology [1]. MOSFET can be employed in an intelligent system of control [2]. Additionally, in the optimization of hybrid energy systems [3]. As channel lengths are reduced to nanoscale scale, SCEs such as threshold voltage (V_{TH}) roll-off, Drain Induced Barrier Lowering (DIBL), and increased leakage currents (I_{OFF}) present significant hurdles to device performance and reliability. These constraints need the development of novel techniques that maintain electrostatic integrity while ensuring elevated drive current and minimal power consumption. Multiple solutions have been suggested, including silicon-on-insulator (SOI) architectures and high-k gate dielectrics. SOI MOSFETs utilize a buried oxide layer to diminish parasitic capacitance and leakage [4,5], although high-k materials like Al_2O_3 (k = 9, Eg = 8.8 eV) and HfO_2 (k = 25, Eg = 5.8 eV) are replacing traditional SiO_2 to facilitate additional scaling [6]. Although these methods have demonstrated efficacy, they mainly depend on global structural changes. Localized dielectric engineering has received insufficient attention, despite its potential to more effectively mitigate SCEs without the disadvantages associated with continuous buried oxides. Narayanan et al. [7] examined the kink effect in partially depleted SOI 2 µm MOSFETs and showed that the implantation of a 0.4 µm SELBOX structure beneath the source and drain efficiently mitigates the floating-body-induced kink. The work demonstrated using Silvaco ATLAS simulations that optimizing the length and thickness of the oxide gap diminishes the kink effect while maintaining the advantages of SOI, with a created device model offering more insights into the optimization of SELBOX parameters. Thakral et al. [8] examined the scaling difficulties of 28 nm SOI MOSFETs and discovered planar fully depleted SOI (FD-SOI) as an appropriate low-power substitute for bulk CMOS. Their TCAD-based research shown that the kink effect in partially depleted SOI (PD-SOI) devices may be effectively mitigated with the implementation of a 0.4 µm SELBOX structure, hence improving device reliability while maintaining the fundamental advantages of SOI technology. Narayanan et al. [9] introduced an enhanced 0.12 µm SOI MOSFET architecture using a 100 nm SELBOX beneath the source and drain to reduce self-heating issue. TCAD simulations validated that adjusting gap parameters significantly mitigates thermal effects while maintaining SOI performance advantages. Mahmoud et al. [10] constructed a 90 nm CMOS employing a 10 nm SELBOX via TCAD ATLAS and assessed the dynamic power relative to SOI CMOS and BULK CMOS. The total dissipated dynamic power across all individuals is equivalent at elevated frequencies. The dynamic power dissipation of the SOI and SELBOX structures was similar at low frequencies, both demonstrating lower values than the BULK configuration. SELBOX CMOS eliminated the kink effect and self-heating, making it superior than SOI CMOS. The SELBOX MOSFET improves device efficiency by reducing power loss. Yoo and Kim [11] introduced a 45 nm buried oxide with a Buried Oxide – Nanosheet Field Effect Transistor (BO-NSFET) that situates the oxide

exclusively beneath the gate region to mitigate substrate band-to-band tunneling (BTBT). TCAD simulations show that this design significantly reduces I_{OFF} and leakage in comparison to conventional Nanosheet Field-Effect Transistors (NSFETs), hence enhancing performance for advanced nodes. Murshid and Bashir [12] presented a ground plane selective buried oxide layer (GP-SELBOX) junction less transistor to address the constraints of traditional SOI-JLTs at sub-20 nm nodes. The incorporation of a p-type ground plane with 10 nm SELBOX resulted in increased depletion, diminished leakage, enhanced I_{ON}/I_{OFF} ratio, and superior SCEs management, while preserving a similar cutoff frequency and reduced self-heating issue.

This study establishes the novelty of SELBOX layer engineering in nanoscale MOSFETs by combining material choice and vertical placement analysis. Unlike conventional strategies, our results reveal that higher-bandgap buried dielectrics such as SiO_2, when positioned closer to the channel-drain junction, can simultaneously suppress leakage current by up to 33% and increase breakdown voltage by more than fivefold compared to the standard design. Al_2O_3 shows moderate improvement, while HfO_2 demonstrates the limitations of using lower-bandgap dielectrics in this role. These findings highlight a previously unexplored design dimension: the coupling between buried dielectric material properties and spatial positioning, which can serve as a new pathway for optimizing short-channel device performance in advanced technology nodes.

2. Methodology

This work simulates and analyzes the nano regime of n-channel MOSFET utilizing TCAD Silvaco ATLAS. The device has a total lateral length of 100 nm and a channel length of 20 nm. The device utilizes a high-k gate dielectric, particularly HfO_2, to minimize gate leakage while preserving robust electrostatic regulation of the channel, as shown in Table 1, which depicts the main parameters [8].

TABLE 1. Parameters of design 20 nm n-MOSFET.

Parameters	Value
Channel	20 nm Si
Doping of Source and Drain	$5 \times 10^{20}\ cm^{-3}$
Doping of Channel	$9 \times 10^{17}\ cm^{-3}$
Doping of Substrate	$1 \times 10^{14}\ cm^{-3}$
Gate Workfunction	4.55ev
Gate length	25 nm
Source and Drain Length	40 nm
Gate Dielectric Thickness	10 nm

In this simulation structure, accurate model selection is essential. This study utilizes the Auger model for direct transitions with three carriers, the SRH model for carrier-fixed minority lifetimes, the Arora model as a replacement for the ANALYTIC model for silicon, and the CVT model for the complete system. The numerical solution technique, Newton-Gummel with trap autonr, frequently yields more precise starting estimates for complex cases.

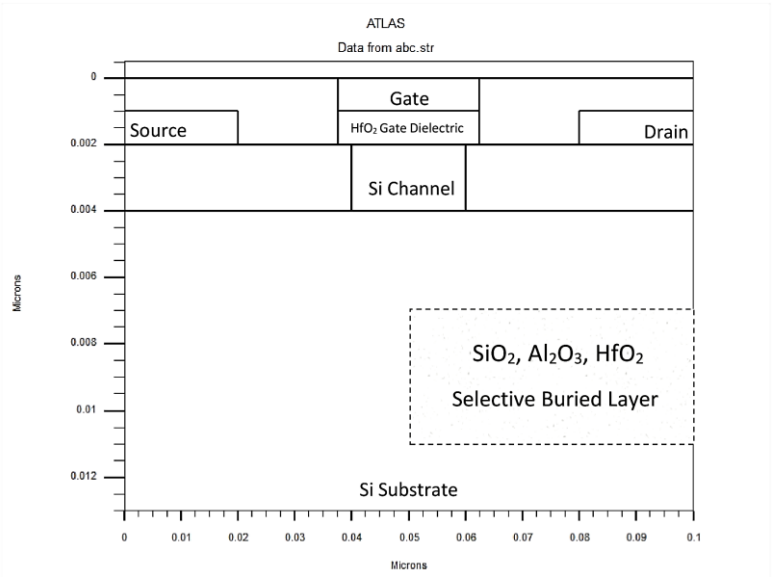

Fig. 1. Schematic View of insertion selective buried oxide layer (SELBOX) in 20 nm n-MOSFET.

An essential element of this study is the incorporation of a selective oxide layer buried into the silicon substrate. The SELBOX is designed to possess a thickness of 40 nm, at 30 nm depth, with its lateral dimensions ranging from 50 nm to 100 nm over the x-axis. Three distinct dielectric materials are utilized independently for the SELBOX in different models: SiO_2, Al_2O_3, and HfO_2 as shown in Figure 1. This facilitates a comparative assessment of the impact of each dielectric material and band gap value on the device concerning SCEs. In succeeding modeling, the SELBOX is elevated in the upward direction until it achieves direct contact with the active channel region. The use of various materials and vertical repositioning is conducted to assess how the closeness of the SELBOX to the channel affects electric field distributions and whole device performance.

3. Results and Discussion

3.1. SiO_2 material (k=3.9 and band gap=9 eV)

This study assesses the electrical properties of 20 nm n-MOSFET devices with SiO_2 SELBOX depths of 30 nm, 20 nm, 10 nm, and direct contact position with the channel, in comparison to a standard design of 20 nm n-MOSFET (without a SELBOX). The primary parameters evaluated comprise threshold voltage (V_{TH}), ON current (I_{ON}), OFF current (I_{OFF}), I_{ON}/I_{OFF} ratio, breakdown voltage, and Drain-Induced Barrier Lowering (DIBL).

Table 2 illustrates that the V_{TH} exhibits remarkable stability across all SELBOX positions, with minimal variations from 0.462 V in the standard design to 0.461 V in the direct contact position, that means the substrate coupling not affected, in order to the electrostatics in the channel stay steady. The slight fluctuation indicates that the vertical placement of the SiO_2 SELBOX minimally affects the V_{TH}, which is beneficial for preserving device switching stability.

TABLE 2. Main parameters of (standard design of n-MOSFET) and the influence of SiO_2 selective buried oxide layer (SELBOX) at (30 nm depth, 20 nm depth, 10 nm depth and direct contact position).

Parameters	Standard	30 nm Depth	20 nm Depth	10 nm Depth	Direct Contact
V_{TH} (V)	0.462	0.454	0.456	0.458	0.461
$I_{ON} \times 10^{-3}$ (A/m)	2	2.12	2.11	2.10	2.07
$I_{OFF} \times 10^{-11}$(A/m)	8.5	10	8.89	7.24	5.68
$I_{ON}/I_{OFF} \times 10^{7}$	2 .37	1.98	2.37	2.90	3.65
Breakdown Voltage (V)	85.09	137.1	199.3	312.5	491.4
DIBL (mV/V)	308	307	306	304	302

The I_{ON} exhibits a little fluctuation with alterations in SELBOX depth. Raising the SELBOX depth from 30 nm to 10 nm improves electrostatic gate control over the channel, elevating I_{ON} from 2.00×10^{-3} A/m in the standard design to 2.12×10^{-3} A/m at 30 nm depth. When the SELBOX is in direct contact with the channel, I_{ON} diminishes to 2.07×10^{-3} A/m, indicating a decline in effective gate control caused by the modified field distribution inside the device's bulk [14].

Conversely, the I_{OFF} has a greater degree of fluctuation. The implanting of a SELBOX at a depth of 30 nm elevates I_{OFF} from 8.5×10^{-11} A/m at standard design to 1.0×10^{-10} A/m at 30 nm depth. This augmentation is ascribed to improved fringing fields at the source/drain regions and supplementary junction leakage resulting from physical separation from the substrate. Notably, placing the SELBOX in direct contact position markedly decreases I_{OFF} to 5.68×10^{-11} A/m, attributable to enhanced isolation and the mitigation of leakage pathways to the substrate [15].

The I_{ON}/I_{OFF} ratio significantly enhances, attaining 3.65×10^7 in the direct contact position, in contrast to 2.37×10^7 in the standard MOSFET. This illustrates exceptional switching performance and indicates that the revised SELBOX positioning improves the equilibrium between I_{ON} performance and I_{OFF} mitigation. A significant enhancement is noted in the breakdown voltage, rising from 85.09 V in the standard design to 491.4 V upon direct contact of the SELBOX with the channel. This improvement results from the diminished fringing fields at the drain side, coupled with the high bandgap (about 9 eV) of SiO_2 and its insulating barrier effect, which decreases the vertical electric field within the substrate and enhances dielectric robustness. As a result, leakage is further reduced, and the MOSFET attains markedly improved dependability [16] [17].

The DIBL values consistently approximate 306 mV/V across all configurations, indicating that the SELBOX placement predominantly influences leakage and breakdown properties rather than electrostatic stability.

Figure 2 depicts the influence of SiO_2 SELBOX positioning on the electric field distribution within the MOSFET structure. At a depth of 30 nm, the SELBOX exhibits a little increase in fringing electric fields on the source side, whereas a more pronounced enhancement is noted on the drain side. The blockage of the field lines by the oxide barrier affects the potential distribution, resulting in localized field crowding around the drain junction. Above the SELBOX on the drain side, the field line density diminishes, indicating partial shielding supplied by the buried oxide layer.

As the SELBOX is raised from a depth of 30 nm to a direct contact position beneath the drain region, the field distribution exhibits significant enhancements. The source side fringing fields have diminished, and the SELBOX now functions as a more robust barrier against electric field entry into the substrate, efficiently directing and reducing substrate coupling. At the drain side, the electric field intensity at the drain-substrate interface becomes higher, while the oxide isolation considerably diminishes field entry into the bulk silicon, thereby

avoiding early breakdown of the device. The enhanced field confinement results in a significant rise in breakdown voltage, as verified by Table 2, which shows breakdown voltage rising from 85.09 V in the standard design to 491.4 V with direct contact to the SELBOX.

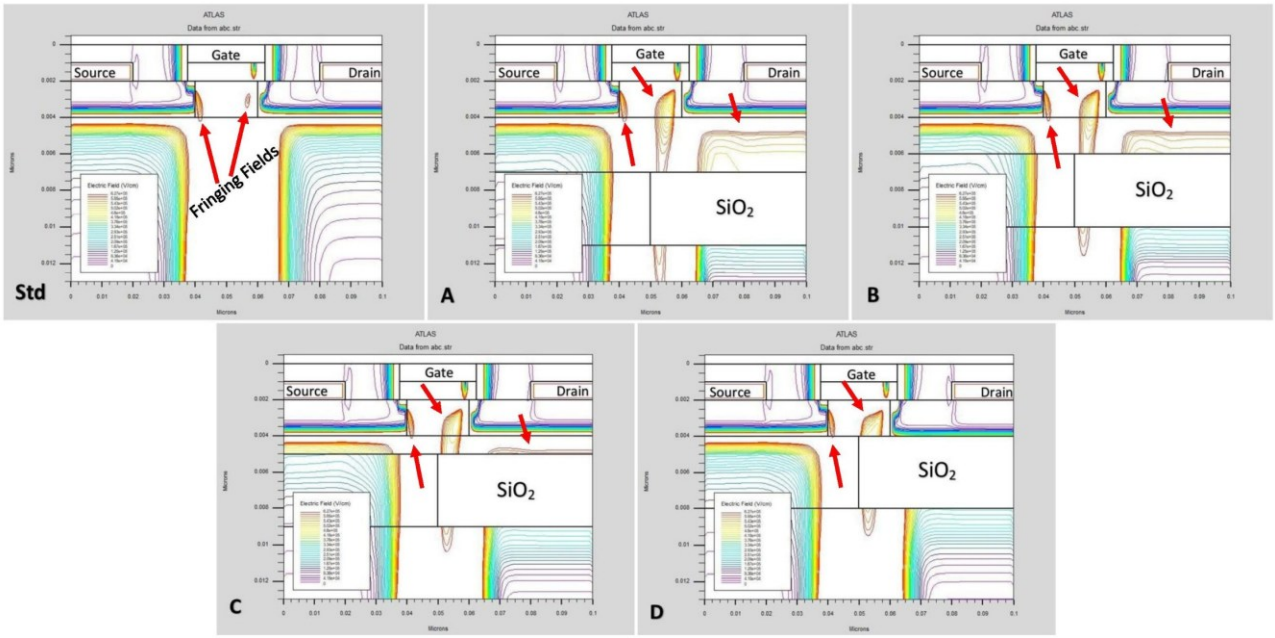

Fig. 2. Electric field distribution at (standard design of n-MOSFET) and SiO_2 selective buried oxide layer (SELBOX) at (30 nm depth, 20 nm depth, 10 nm depth and direct contact position).

3.2. Al_2O_3 material (k=9 and band gap=8.8 eV)

This investigation assesses the performance of MOSFET devices utilizing Al_2O_3 as the SELBOX at depths of 30 nm, 20 nm, 10 nm, and in direct contact with the channel, in comparison to a conventional design.

Table 3 demonstrates that the V_{TH} exhibits exceptional stability, with values fluctuating between 0.461 V and 0.464 V across all SELBOX designs. This slight difference verifies that Al_2O_3 SELBOX has no negative effect on channel electrostatics or gate control. The elevated dielectric constant (k = 9) of Al_2O_3 facilitates enhanced gate-to-channel modulation while effectively mitigating SCEs. The stability of V_{TH} emphasizes Al_2O_3's capacity to deliver reliable switching behavior, essential for sophisticated CMOS design.

The I_{ON} performance is robust and stable, exhibiting only slight fluctuations compared to the standard design. At all SELBOX depths, including direct contact, the I_{ON} remains stable with 2.0×10^{-3} A/m , indicating that Al_2O_3's elevated dielectric constant maintains effective electrostatic gate control, even when the oxide layer is relocated nearer to the drain region. This differs from SiO_2 SELBOX findings, where a minor decrease in I_{ON} was noted at direct contact, highlighting Al_2O_3's advantage in preserving robust inversion charge density and I_{ON} capacity.

The I_{OFF} exhibits a distinct decline as the SELBOX is raised from 8.52×10^{-11} A/m at a depth of 30 nm to 6.20×10^{-11} A/m at direct contact position. This enhancement is ascribed to diminished fringing electric fields next to the drain junction and improved physical separation of leakage pathways between the source/drain and the substrate.

The I_{ON}/I_{OFF} ratio markedly increases from 2.37 x 10^7 in the standard design to 3.24×10^7 upon direct contact position, indicating enhanced switching efficiency with minimal reduction in I_{ON}.

The breakdown voltage significantly increases from 85.09 V in the standard design to 275.7 V in the direct contact position of SELBOX. This enhancement arises from the high-k insulating Al_2O_3 layer, which diminishes vertical electric field leakage into the substrate and improves junction isolation. Despite Al_2O_3 having a bandgap of around 8.8 eV, which is marginally lower than SiO_2's bandgap of about 9 eV, it remains effective in mitigating high-field stress and junction leakage. The modest rise in breakdown voltage relative to SiO_2 based SELBOX configurations emphasizes the significance of dielectric bandgap and permittivity trade-offs. Al_2O_3 marginally diminishes leakage and substantially enhances breakdown voltage, however not to the same degree as SiO_2 SELBOX.

DIBL remains approximately consistent at 308 mV/V across all configurations, indicating that variations in SELBOX position and oxide material selection predominantly influence leakage and breakdown performance rather than the integrity of electrostatic gate channel control.

TABLE 3. Main parameters of (standard design of n-MOSFET) and the influence of Al_2O_3 selective buried oxide layer (SELBOX) at (30 nm depth, 20 nm depth, 10 nm depth and direct contact position).

Parameters	Standard	30 nm Depth	20 nm Depth	10 nm Depth	Direct Contact
V_{TH} (V)	0.462	0.461	0.462	0.463	0.464
$I_{ON} \times 10^{-3}$ (A/m)	2	2.03	2.03	2.02	2.01
$I_{OFF} \times 10^{-11}$(A/m)	8.5	8.52	7.97	7.25	6.20
$I_{ON}/I_{OFF} \times 10^7$	2 .37	2.38	2.53	2.79	3.24
Breakdown Voltage (V)	85.09	130.5	155.7	198.7	275.7
DIBL (mV/V)	308	308	307	307	306

Figure 3 depicts the alterations in the electric field profile resulting from the relocation of the Al_2O_3 SELBOX. At a depth of 30 nm, the SELBOX induces a minor enhancement of fringing fields on the drain side, attributable to localized field crowding near the drain junction. As the SELBOX is elevated nearer to the drain, surrounding fields diminish consistently, exhibiting substantial suppression at the position of direct contact. The electric field scattering over the Al_2O_3 SELBOX is practically eliminated, illustrating the oxide's excellent insulating capability.

The reallocation of field lines increases device durability by diminishing vertical field penetration into the substrate, thereby decreasing leakage routes and enhancing breakdown voltage. The capability of Al_2O_3 SELBOX to sustain minimal I_{OFF} while ensuring field confinement makes it exceptionally advantageous for scaled MOSFET topologies, particularly in scenarios where oxide engineering is essential for optimizing I_{ON}, I_{OFF}, and device reliability.

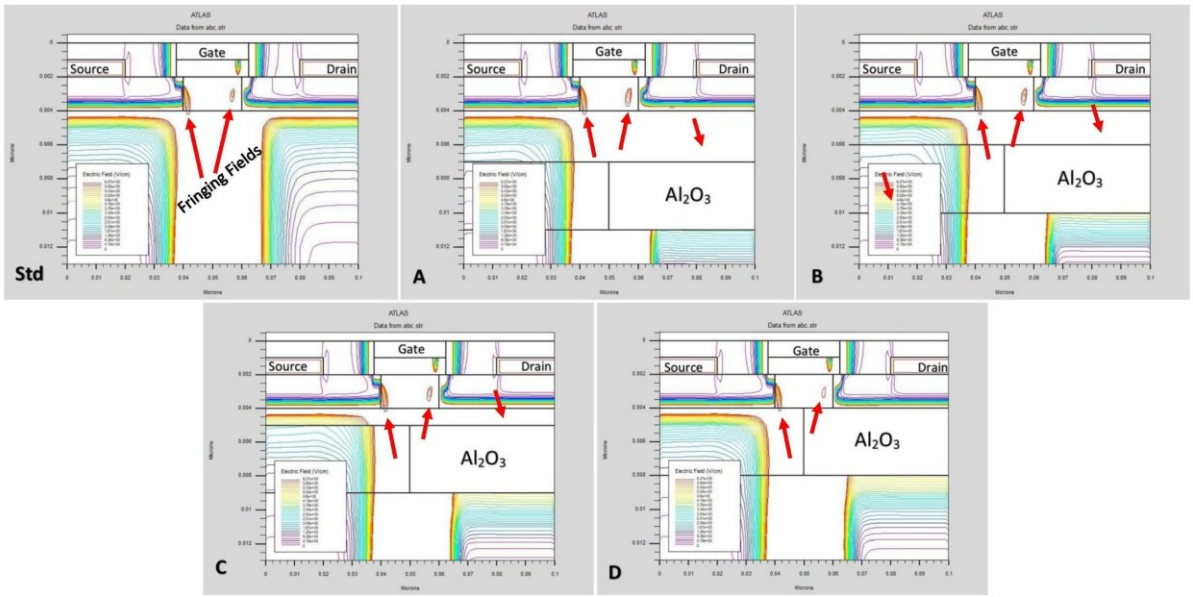

Fig. 3. Electric field distribution at (standard design of n-MOSFET) and Al_2O_3 selective buried oxide layer (SELBOX) at (30 nm depth, 20 nm depth, 10 nm depth and direct contact position).

3.3. HfO_2 material (k=25 and band gap=5.8 eV)

This section examines the influence of different HfO_2 SELBOX depths 30 nm, 20 nm, and 10 nm, along with a direct contact configuration, on the performance of MOSFET devices, compared to a standard design of MOSFET device.

Table 4 depicts that the V_{TH} exhibits a slight elevation with the implementation of the HfO_2 SELBOX, increasing from 0.462 V in the standard design to a peak of 0.470 V when the SELBOX is situated 30 nm beneath the drain region. The increase results from improved electrostatic confinement and less substrate coupling facilitated by the high-k HfO_2 layer, which reduces gate control over the channel at intermediate depths. As the SELBOX is elevated nearer to direct contact with the drain, V_{TH} marginally lowers to 0.464 V. This reduction signifies that, although HfO_2 improves vertical isolation, its closeness to the channel somewhat modifies the electric field distribution and diminishes gate-to-channel electrostatics, resulting in a modest decrease in V_{TH} [18].

The I_{ON} values are marginally diminished in comparison to the standard MOSFET structure with 2.00×10^{-3} A/m. The values fluctuate between 1.93×10^{-3} A/m and 1.97×10^{-3} A/m across all structures. The decrease is ascribed to the elevated dielectric constant and physical thickness of the SELBOX, which marginally diminishes inversion charge density and channel mobility by altering vertical electric fields. The little decrease in I_{ON} suggests that the integration of HfO_2 SELBOX entails a compromise in I_{ON} performance.

The I_{OFF} demonstrates a nonlinear pattern. Initially, it diminishes to 7.44×10^{-11} A/m at a SELBOX depth of 30 nm, due to diminished substrate coupling and efficient obstruction of leakage pathways. As the SELBOX approaches direct contact, I_{OFF} increases to 10.3×10^{-11} A/m, attributed to improved field penetration through the reduced substrate regions and leakage pathways along the SELBOX peripheries.

The I_{ON}/I_{OFF} ratio exhibits a trend, reaching a maximum of 2.61×10^7 at a depth of 30 nm, exceeding the standard design of 2.37×10^7, before decreasing to 1.91×10^7 upon direct contact position. The results indicate that a 30 nm SELBOX depth optimally suppresses leakage while sustaining acceptable I_{ON} levels, whereas direct contact, while enhancing breakdown voltage, and increases I_{OFF}.

The breakdown voltage markedly increases with the incorporation of HfO_2 SELBOX, rising from 85.09 V at standard design to 172.3 V direct contact position. This improvement is due to HfO_2's elevated dielectric constant and its physical barrier effect, which diminishes vertical electric field intensity in the bulk substrate, hence enhancing device stability. In contrast to SiO_2 SELBOX, HfO_2's reduced bandgap (about 5.8 eV versus 9 eV) restricts the enhancement of maximum breakdown voltage and results in elevated I_{OFF}, especially when the oxide is situated in proximity to the drain region.

DIBL exhibits relative stability across all SELBOX depths at around 312 mV/V, indicating that although the selection and positioning of SELBOX materials significantly affect leakage and breakdown properties, electrostatic channel management remains uniform.
7.44×10^{-11} A/m at a SELBOX depth of 30 nm, subsequently rising to 10.3×10^{-11} A/m as the SELBOX's direct contact position is altered. This increase is attributed to the SELBOX facilitating leakage pathways between the source and drain regions and the substrate. The I_{ON}/I_{OFF} ratio attains its maximum at a depth of 30 nm, measuring 2.61×10^7, above the conventional design value of 2.37×10^7. However, it progressively decreases as the SELBOX is moved to the direct contact position, ultimately reaching 1.91×10^7. In comparison to the conventional MOSFET design, the breakdown voltage increases from 85.09 V to 172.3 V when a SELBOX is implanted at the direct contact location. The SELBOX first increases the breakdown voltage by creating an insulating barrier that reduces the vertical electric field in the bulk substrate. When the value of the band gap value became half of the band gap in first case, about 5.8 eV, and becoming closer

to the drain region, leading to a slight increment in the breakdown voltage, and an increase in the leakage current. DIBL values almost constant for all cases is approximately about 312 mV/V.

TABLE 4. Main parameters of (standard design of n-MOSFET) and the influence of HfO_2 selective buried oxide layer (SELBOX) at (30 nm depth, 20 nm depth, 10 nm depth and direct contact position).

Parameters	Standard	30 nm Depth	20 nm Depth	10 nm Depth	Direct Contact
V_{TH} (V)	0.462	0.470	0.468	0.466	0.464
$I_{ON} \times 10^{-3}$ (A/m)	2	1.94	1.95	1.93	1.97
$I_{OFF} \times 10^{-11}$(A/m)	8.5	7.44	8.76	10	10.3
$I_{ON}/I_{OFF} \times 10^{7}$	2 .37	2.61	2.22	1.95	1.91
Breakdown Voltage (V)	85.09	111.6	109.1	125.3	172.3
DIBL (mV/V)	308	311	312	314	314

Figure 4 clarifies the characteristics of the electric field. The integration of HfO_2 SELBOX at a depth of 30 nm markedly diminishes fringing fields adjacent to the drain side, while the high-k shielding action of the oxide effectively obstructs field lines above the SELBOX. As the SELBOX approaches direct contact with the drain, the confinement of the electric field enhances, resulting in less vertical field penetration into the substrate. Nevertheless, robust localized electric fields develop within the SELBOX layer, aligning with the noted rise in I_{OFF}. This indicates that although HfO_2's elevated dielectric constant enhances isolation, its reduced bandgap renders it more vulnerable to field-assisted leakage mechanisms in comparison to SiO_2 or Al_2O_3 SELBOX.

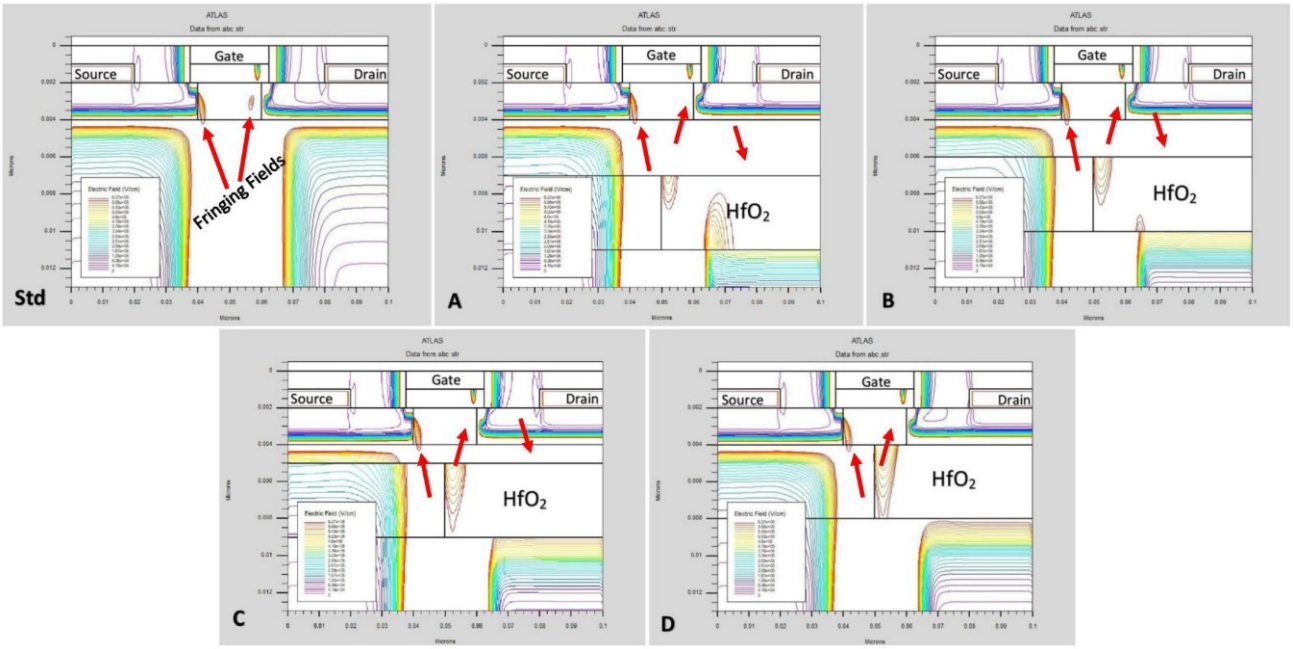

Fig. 4. Electric field distribution at (standard design of n-MOSFET) and HfO_2 selective buried oxide layer (SELBOX) at (30 nm depth, 20 nm depth, 10 nm depth and direct contact position).

4. Conclusion

Implanting a SELBOX beneath of drain region with three different materials, SiO_2, Al_2O_3, and HfO_2, with energy gaps of 9 eV, 8.8 eV, and 5.8 eV, respectively. The value of energy gap of materials and its closeness to drain region determines the average increasing and decreasing value of leakage current and breakdown voltage, as the SELBOX positioning from 30 nm depth to direct contact, it was noticed when the high value of band gap, such SiO_2 with 9 eV, and become more close to the drain-substrate contact, the leakage current is exponentially decreased by 17%, and the breakdown voltage is exponentially increased by 52%. When the band gap is slightly decreased, such as Al_2O_3 with 8.8 eV, the leakage current is slightly exponentially decreased by 10%, and the breakdown voltage is exponentially increased by 29%. Finally, the significant decrease in the value of band gap, such as HfO_2 with 5.8 eV, the leakage current is exponentially increased by 17%, and the breakdown voltage is exponentially increased by 16%. It was concluded that the material with a higher value of the band gap and closer to the drain region gives better results. Future research can extend this work in several directions, like exploring alternative high-k and ultra-wide band gap dielectrics such as ZrO_2, La_2O_3, or Ga_2O_3 as SELBOX layers could provide further insights into material-dependent performance. Another future approach, applying the concept of buried dielectric engineering to advanced device architectures, including FinFETs, Gate-All-Around (GAA) FETs, and nanosheet transistors, may reveal its scalability to beyond-20 nm nodes.

References

[1] M. Aditya, K. S. Rao, B. Balaji, and K. G. Sravani, "Comparison of drain current characteristics of advanced MOSFET structures-a review," *Silicon,* vol. 14, no. 14, pp. 8269-8276, 2022. https://doi.org/10.1007/s12633-021-01638-8

[2] R. H. Ahmed and A. S. Nouri, "Enhanced Transient Stability in Power Systems via Intelligent Control of SVCs Using Neural Networks," *Electrical Engineering Technical Journal,* vol. 2, no. 2, pp. 17-24, 2025. https://doi.org/10.51173/eetj.v2i2.23

[3] S. M. Ferhan and H. Agahi, "Multi-Objective Optimization of Hybrid Energy Systems," *Electrical Engineering Technical Journal,* vol. 2, no. 2, pp. 1-16, 2025. https://doi.org/10.51173/eetj.v2i2.22

[4] K. Pradhan, P. Agarwal, P. Sahu, and S. Mohapatra, "Role of high-k materials in Nanoscale TM-DG MOSFET: A simulation study," *Invertis Journal of Science & Technology,* vol. 6, no. 4, pp. 195-199, 2013.

[5] B. Majkusiak, T. Janik, and J. Walczak, "Semiconductor thickness effects in the double-gate SOI MOSFET," *IEEE Transactions on Electron Devices,* vol. 45, no. 5, pp. 1127-1134, 2002. https://doi.org/10.1109/16.669563

[6] H. Yu *et al.*, "Energy gap and band alignment for (HfO 2) x (Al 2 O 3) 1− x on (100) Si," *Applied Physics Letters,* vol. 81, no. 2, pp. 376-378, 2002. https://doi.org/10.1063/1.1492024

[7] M. Narayanan, H. Al-Nashash, B. Mazhari, D. Pal, and M. Chandra, "Analysis of kink reduction in SOI MOSFET using selective back oxide structure," *Active and Passive Electronic Components,* vol. 2012, no. 1, p. 565827, 2012. https://doi.org/10.1155/2012/565827

[8] B. Thakral, G. Bakshi, and A. K. Kushwaha, "A review on SOI MOSFET and kink reduction using selective back oxide structure," in *2014 International Conference on Reliability Optimization and Information Technology (ICROIT)*, 2014: IEEE, pp. 487-490. https://doi.org/10.1109/ICROIT.2014.6798372

[9] M. Narayanan and H. Al Nashash, "Minimization of self-heating in SOI MOSFET devices with SELBOX structure," in *2016 11th International Conference on Advanced Semiconductor Devices & Microsystems (ASDAM)*, 2016: IEEE, pp. 61 https://doi.org/10.1109/ASDAM.2016.7805895

[10] R. Mahmoud, N. Madathumpadical, and H. Al-Nashash, "TCAD simulation and analysis of selective buried oxide MOSFET dynamic power," *Journal of Low Power Electronics and Applications,* vol. 9, no. 4, p. 29, 2019. https://doi.org/10.3390/jlpea9040029

[11] S. Yoo and S. Kim, "Leakage optimization of the buried oxide substrate of nanosheet field-effect transistors," *IEEE Transactions on Electron Devices,* vol. 69, no. 8, pp. 4109-4114, 2022. https://doi.org/10.1109/TED.2022.3182300

[12] M. Murshid and F. Bashir, "Ground plane and selective buried oxide based planar junctionless transistor," *Frequenz,* vol. 76, no. 1-2, pp. 1-7, 2022. https://doi.org/10.1515/freq-2021-0059

[13] V. P. Tayade and S. L. Lahudkar, "Implementation of 20 nm graphene channel field effect transistors using silvaco TCAD tool to improve short channel effects over conventional MOSFETs," *Advances in Technology Innovation,* vol. 7, no. 1, pp. 18-29, 2021. https://doi.org/10.46604/aiti.2021.8098

[14] J.-T. Park and J.-P. Colinge, "Multiple-gate SOI MOSFETs: device design guidelines," *IEEE transactions on electron devices,* vol. 49, no. 12, pp. 2222-2229, 2002. https://doi.org/10.1109/TED.2002.805634

[15] T. Ernst, R. Ritzenthaler, O. Faynot, and S. Cristoloveanu, "A model of fringing fields in short-channel planar and triple-gate SOI MOSFETs," *IEEE transactions on electron devices,* vol. 54, no. 6, pp. 1366-1375, 2007. https://doi.org/10.1109/TED.2007.895241

[16] A. Aminbeidokhti, A. A. Orouji, S. Rahmaninezhad, and M. Ghasemian, "A novel high-breakdown-voltage SOI MESFET by modified charge distribution," *IEEE transactions on electron devices,* vol. 59, no. 5, pp. 1255-1262, 2012. https://doi.org/10.1109/TED.2012.2186580

[17] D. Madadi, A. A. Orouji, and A. Abbasi, "Improvement of nanoscale SOI MOSFET heating effects by vertical Gaussian drain-source doping region," *Silicon,* vol. 13, no. 3, pp. 645-651, 2021. https://doi.org/10.1007/s12633-020-00453-x

[18] M. G. C. de Andrade and J. A. Martino, "Threshold voltages of SOI MuGFETs," *Solid-State Electronics,* vol. 52, no. 12, pp. 1877-1883, 2008. https://doi.org/10.1016/j.sse.2008.06.046